SINGLE WIRE INTERFACE FOR LCD CALIBRATOR

FIELD OF THE INVENTION

[0001] This invention relates generally to liquid crystal displays (LCDs), and in particular, to a single wire interface for an LCD calibrator.

BACKGROUND OF THE INVENTION

[0002] The production of LCDs typically entails manufacturing the LCDs, and subsequently testing and adjusting LCDs. During the testing and adjustment of the LCDs panels, various parameters of the LCDs are adjusted to fine tune the displaying operation of the LCDs. One such parameter, in particular, is the common electrode voltage Vcom of the LCDs. As is explained below with reference to Figure 1, the common electrode voltage Vcom affects the display characteristics of an LCD, including the flicker characteristic.

[0003] Figure 1 illustrates a block diagram of a typical LCD 100. The LCD 100 consists of a data signal line driver 102 to generate data voltages for pixels in common columns respectively by way of a plurality of data lines (DL#). The LCD 100 further consists of a scan signal line driver 104 to generate select line voltages for pixels in common rows respectively by way of a plurality of select lines (SL#). Each pixel 106 consists of a field effect transistor (FET) having a gate (G) electrically coupled to the corresponding select line, a drain (D) electrically coupled to the corresponding data line, and a source (S) electrically coupled to a segment electrode of a liquid crystal (LC) medium. A common electrode voltage Vcom, common to all of the pixels, is applied to a common electrode of the LC medium.

[0004] The LCD 100 further consists of a common electrode voltage adjustment circuit 108 consisting of a voltage divider including resistor R1 and variable resistor R2 connected in series between a supply voltage Vcc and ground. The intermediate node between the resistors

R1 and R2 is coupled to a buffer 110 to generate the common electrode voltage Vcom.

[0005] During a frame cycle, the scan signal line driver 104 sequentially activates the select lines (SL) to respectively display the frame lines. For each activated select line (SL), the data signal line driver 102 activates the data lines (DL) depending on which pixels are to be activated based on the input image data. A pixel is activated if both the corresponding select line (SL) and corresponding data line (DL) are activated, causing the corresponding FET to turn "on", thereby generating a current through the liquid medium (LC).

[0006] As previously discussed, the common electrode voltage Vcom affects the illumination characteristics of the pixels, such as the flicker characteristics. During testing, a technician manually adjusts the resistor R2 to set the desired common electrode voltage Vcom voltage while monitoring a test pattern displayed by the LCD. Once the desired common electrode voltage Vcom is set and all other parameters are tested and adjusted, the LCD unit is securely packaged and future access to such adjustments are not typically undertaken due to difficulties in obtaining access to such components after the LCD unit is securely packaged.

[0007] Accordingly, it is desirable to provide an interface which facilitates the electronic adjustment of such parameters. In addition, it is further desirable that such an interface include as minimal contacts for coupling to an external programming unit.

SUMMARY OF THE INVENTION

[0008] An aspect of the invention relates to a calibration circuit for adjusting a common electrode voltage Vcom of a liquid crystal display (LCD) in response to commands received by way of a single-wire interface. The calibration circuit includes a controller to receive and interpret commands in the form of positive and negative pulses for increasing and decreasing the common electrode voltage Vcom by a

predetermined amount per pulse. The calibration circuit includes a counter for generating a count related to the Vcom, wherein the controller causes the count to increment and decrement in response to the negative and positive command pulses. The calibration circuit further includes a non-volatile memory for storing the count, wherein the controller causes the count to be stored into the non-volatile memory in response to another command in the form of a voltage above a predetermined threshold. This voltage is also used for programming the non-volatile memory.

[0009] Another aspect of the invention relates to method of adjusting a common electrode voltage, Vcom of a liquid crystal display (LCD), comprising receiving a first command to increase the common electrode voltage Vcom by way of a single-wire interface; increasing the common electrode voltage Vcom in response to the first command; receiving a second command to decrease the common electrode voltage Vcom by way of the single-wire interface; and decreasing the common electrode voltage Vcom in response to the second command. This method may further entail receiving a third command to store a count related to the common electrode voltage Vcom in a non-volatile memory by way of the single-wire interface; and storing the count in the non-volatile memory in response to the third command.

[0010] Other aspects, features and techniques will become apparent to one skilled in the relevant art in view of the following detailed description of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 illustrates a block diagram of a typical LCD;

[0012] Figure 2 illustrates a block diagram of an exemplary LCD in accordance with an embodiment of the invention;

[0013] Figure 3 illustrates a block diagram of an exemplary calibration interface circuit in accordance with another embodiment of the invention; and

[0014] Figure 4 illustrates a timing diagram of the command signals associated with the exemplary calibration circuit in accordance with another aspect of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Figure 2 illustrates a block diagram of an exemplary LCD 200 in accordance with an embodiment of the invention. The LCD 200 comprises a data signal line driver 202 to generate data voltages for pixels in common columns respectively by way of a plurality of data lines (DL#). The LCD 200 further comprises a scan signal line driver 204 to generate select line voltages for pixels in common rows respectively by way of a plurality of select lines (SL#). Each pixel 206 comprises a switching element such as FET having a gate (G) electrically coupled to the corresponding select line, a drain (D) electrically coupled to the corresponding data line, and a source (S) electrically coupled to a segment electrode of a liquid crystal (LC) medium. A common electrode voltage Vcom, common to all of the pixels, is applied to a common electrode of the LC medium.

[0016] As discussed in the Background section, the common electrode voltage Vcom affects the illumination characteristics of the pixels, such as the flicker characteristics. Accordingly, for adjusting the common electrode voltage Vcom, the exemplary LCD 200 further comprises a calibration interface circuit 210 having an interface to receive external commands for programming the common electrode voltage Vcom, and an output for generating the common electrode voltage Vcom. As is discussed in further detail below, the calibration interface circuit 210 receives a set of commands for adjusting the common electrode voltage Vcom, and another command for causing the desired level for the common electrode voltage Vcom to be rewritten to a non-volatile memory. In the exemplary embodiment, the calibration interface circuit 210 receives these commands by way of a single-wire interface.

[0017] Figure 3 illustrates a block diagram of an exemplary calibration interface circuit 300 in accordance with another embodiment of the invention. The calibration interface circuit 300 comprises a controller 302, an up/down counter 304, a non-volatile memory such as the electrically erasable programmable read only memory (EEPROM) 306,

a digital-to-analog converter (DAC) 308, an under voltage lock out (UVLO) circuit 310, comparators 312 and 314, buffer 316, a field effect transistor (FET) 320, and a plurality of resistors R21-R26. These elements of the calibration interface circuit 300 may be packaged as a single integrated circuit 330.

[0018] The exemplary calibration interface circuit 300 further comprises an electrostatic discharge (ESD) protection circuit 324 configured as a low pass filter having a resistor R21 and a capacitor C2, a calibrator enable (CE) circuit 326 including resistor R32, a buffer 322, a voltage divider including resistors R28 and R29, a current-setting resistor R30, and a plurality of bias line filtering capacitors C1 and C3. These elements of the calibration interface circuit 300 may be connected externally to the integrated circuit 330.

[0019] The controller 302 includes a control input (CTL) to receive commands from an external programming unit 400. The ESD protection circuit 324 is electrically connected between the control input (CTL) of the controller 302 and the programming unit 400. More specifically, the resistor R21 is connected in series between the programming unit 400 and the control input (CTL) of the controller 302, and the capacitor C2 is connected in shunt. As is explained in more detail as follows, the ESD protection circuit 324, being configured as a low pass filter, improving the ESD protection.

[0020] The control input (CTL) of the controller 302 is also electrically connected to the intermediate node of a voltage divider comprising resistors R21 and R22 connected between a first supply voltage terminal V_{DD} and a ground terminal. In addition, the control input (CTL) of the controller 302 is electrically connected to the positive input of the comparator 312 via the intermediate node of a voltage divider comprising resistors R23 and R24 connected between the control input (CTL) of the controller 302 and a ground terminal. The control input (CTL) is also electrically connected to the programming input (PROG) of the EEPROM 306. The first supply voltage terminal V_{DD} is electrically

connected to the negative input of the comparator 312. The output of the comparator 312 is electrically connected to the write input (WRITE) of the controller 302, and to the shunt resistor R25 serving as a load for the comparator 312.

[0021] As is explained in more detail as follows, the voltage divider comprising R21 and R22 is used to set a particular voltage on the positive input of the comparator 312 when there is no signal on the control input (CTL). This biases the CTL voltage at $V_{DD}/2$ when there is no signal on the control input (CTL). The voltage divider comprising resistors R23 and R24 is used to set a minimum voltage on the control input (CTL) of the controller 302 which causes the output of the comparator 312 to be asserted. In this example, the minimum control voltage (CTL) is approximately 1.2 V_{DD}.

[0022] The enable input (ENABLE) of the controller 302 is electrically connected to the output of comparator 314. The comparator 314 includes a negative input to receive a predetermined threshold voltage V_{TH}. The comparator 314 includes a positive input to receive a controller enable (CE) signal. When the controller enable (CE) signal is greater than the threshold voltage V_{TH}, the output of the comparator 314 is asserted, thereby asserting the enable input (ENABLE) of the controller 302. When the enable input (ENABLE) of the controller 302 is asserted, the controller 302 responds to commands received via the control input (CTL) for programming the common electrode voltage Vcom. When the enable input (ENABLE) of the controller 302 is not asserted, the controller 302 does not respond to commands received via the control input (CTL) for programming the common electrode voltage Vcom.

[0023] The controller enable (CE) may be tied to the first supply voltage terminal V_{DD} (e.g. $V_{DD} > V_{TH}$) using a jumper to maintain the enable input (ENABLE) of the controller 302 asserted to continuously enable the controller 302 for programming the common electrode voltage Vcom. In addition, the controller enable (CE) may be tied to a ground terminal

by way of resistor R32 using a jumper to maintain the enable input (ENABLE) of the controller 302 non-asserted to continuously disable the controller 302 from programming the common electrode voltage Vcom. This may be useful to prevent the programming of the common electrode voltage Vcom by unauthorized parties.

[0024] The up/down counter 304 includes a clock input (CLK) to receive a clock signal from the controller 302, which is used as a timing signal to sequentially change the count of the up/down counter 304. The up/down counter 304 also includes an up/down input (U/D) 304 to receive a counting direction signal from the controller 302. In addition, the up/down counter 304 also includes a read/write input (R/W) from the controller 302 to selectively fix the count so that it can be written to the EEPROM 306. Additionally, the up/down counter 304 includes a power-on-reset input (POR) to receiver a POR signal which causes the counter 304 to load an input count from the EEPROM 306. Further, the up/down counter 304 includes a count output, coupled to the DAC 308 and the EEPROM 306, to produce the current count. Moreover, the up/down counter 304 includes a count input, coupled to the EEPROM 306, to receive the input count from the EEPROM 306.

[0025] The EEPROM 306 includes a read/write input (R/W) to receive the read/write signal from the controller 302 for selectively enabling the EEPROM 306 for storing the current count generated by the up/down counter 304. The EEPROM 306 further includes a programming input (PROG) to receive a programming voltage from the programming unit 400. The EEPROM 306 further includes an input to receive the current count from the up/down counter 304. And, the EEPROM 306 includes an output to provide the stored count to the count input of the up/down counter 304.

[0026] The DAC 308 includes an input to receive the current count from the up/down counter 304, and an output to generate a voltage related to the current count. The DAC 308 may use a typical resistor ladder, as represented by resistor R27, to generate the count-related voltage. The

resistor ladder R27 is electrically coupled at a first end to a second supply voltage terminal V_{ADD} by way of a resistor R26 and a switch SW, and at a second end to a ground terminal.

[0027] The buffering operational amplifier 316 includes a positive input electrically coupled to the output of the DAC 308, a negative input electrically connected to the source of FET 320 and to current-setting resistor R30 connected to a ground terminal, and an output electrically connected to the gate of FET 320. The drain of FET 320 is electrically connected to the positive input of buffering operational amplifier 322, and to the intermediate node of a voltage divider comprising resistors R28 and R29 connected in series between the second supply voltage terminal V_{ADD} and a ground terminal. The buffering operational amplifier 322 includes a negative input connected to its output, as is customary for an operational amplifier configured as a buffer. The common electrode voltage Vcom of the LCD is generated at the output of the operational amplifier 322.

[0028] The UVLO 310 includes an output to control switch SW and also includes a plurality of outputs to provide a bias voltage to each of the operational amplifiers 312, 314, and 316. The UVLO senses an under voltage of the supply voltage V_{DD}, and opens switch SW if the supply voltage V_{DD} is below a certain threshold. This has the effect of shutting down the operational amplifiers, thereby placing the calibration interface circuit 300 in a low power mode. The shunt-connected capacitors C1 and C3 function is to reduce noise present respectively on the first and second supply voltage terminals V_{DD} and V_{ADD}.

[0029] With reference to Figure 4 which illustrates a timing diagram of the command signals associated with the exemplary calibration circuit 300, the programming unit 400 generates a command to increase the common electrode voltage Vcom by an amount corresponding to a single count in the form of a relatively high voltage pulse having a maximum amplitude above a command-indicating threshold (e.g. $> V_{DD}/2$), a width larger than a predetermined pulse width (e.g. >200 microseconds), and

a maximum amplitude lower than the programming voltage threshold (e.g. 1.2 V_{DD}). Similarly, the programming unit 400 generates a command to decrease the common electrode voltage Vcom by an amount corresponding to a single count in the form of a relatively low voltage pulse having a minimum amplitude below the command-indicating threshold (e.g. $<V_{DD}/2$), a width larger than a predetermined pulse width (e.g. >200 microseconds), and a maximum amplitude lower than the programming voltage threshold (e.g. 1.2 V_{DD}).

[0030] Further, the programming unit 400 generates a command to write the current count of the up/down counter 304 to the EEPROM 306 in the form of a voltage greater than a predetermined threshold (e.g. 1.2 V_{DD}). That command voltage also serves as the programming voltage for the EEPROM 306 which has a specific voltage and timing consideration (e.g. ramp up from 7.75V to 15.5 V within 4 milliseconds, maintain 15.5V for 1 millisecond, and ramp down to $V_{DD}/2$ within 100-1000 microseconds).

[0031] Taking the example given in Figure 4 and with reference to Figure 3, assume the count of the up/down counter 304 is at 64 after a power-on-reset (POR). In addition, it is further assumed that the controller enable (CE) signal is asserted so that the controller 302 responds to programming commands.

[0032] First, the programming unit 400 generates a command to increase the common electrode voltage Vcom by an amount corresponding to a single count. As shown, this command is in the form of a relatively high voltage pulse with a width greater than 200 microseconds and with a maximum amplitude of less than 1.2^*V_{DD}. In response to this command, the controller 302 disasserts the U/D signal so that the up/down counter 304 decrements the count in response to the clock signal generated by the controller 302. Thus, in response to such relatively high voltage pulse, the count changes from 64 to 63. The lower count causes the DAC 308 to generate a corresponding lower voltage. This lower voltage translates into a lower current through the

current-setting resistor R30 due to the operation of the buffer 316 and FET 320 as a current-steering circuit. The lower current causes less voltage drop across resistor R28, thereby causing the common electrode voltage Vcom to increase.

[0033] Second, the programming unit 400 generates a command to decrease the common electrode voltage Vcom by an amount corresponding to a single count. As shown, this command is in the form of a relatively low voltage pulse with a width greater than 200 microseconds and with a maximum amplitude of less than 1.2 V_{DD}. In response to this command, the controller 302 asserts the U/D signal so that the up/down counter 304 increments the count in response to the clock signal generated by the controller 302. Thus, in response to such relatively low voltage pulse, the count changes from 63 to 64. The higher count causes the DAC 308 to generate a corresponding higher voltage. This higher voltage translates into a higher current through the current-setting resistor R30 due to the operation of the buffer 316 and FET 320 as a current-steering circuit. The higher current causes more voltage drop across resistor R28, thereby causing the common electrode voltage Vcom to decrease.

[0034] In the same manner described above, the following two relatively high voltage pulses decrease the count value by two to 62, thereby increasing the common electrode voltage Vcom by an amount corresponding to two counts. Then, according to the example of Figure 4, the following relatively high (e.g. < 20 microseconds) and narrow voltage pulse (which could be noise or interference) has a width less than the requisite minimum pulse width to be recognized as a command. In this case, the controller 302 does not recognize it as a command. This applies also to the following relatively low and narrow voltage pulse. Thus, for these two pulses the count remains at 62, and consequently, the common electrode voltage Vcom remains substantially fixed during this time interval. The relatively narrow

voltage pulses are followed by relatively low and high programming pulse.

[0035] Once the desired common electrode voltage Vcom has been reached, the EEPROM 306 may be programmed to store the count of the up/down counter 304, which corresponds to the desired common electrode voltage Vcom. To accomplish this, the programming unit 400 initially produces a voltage greater than the predetermined threshold of $1.2*V_{DD}$ (e.g. 7.75 V). The programming voltage, being greater than the predetermined threshold, causes the output of the comparator 312 to be asserted. The asserted write input (WRITE) of the controller 302 causes the controller to assert the R/W output, thereby enabling the up/down counter 304 and the EEPROM 306 for programming the count into the EEPROM 306. Then, the programming voltage continues to increase to, for example, 15.5 V, where it is applied to the programming input of the EEPROM 306 for programming the same with the count.

[0036] There are many advantages to the calibration interface circuit 300. First, it provides for the digital tuning of the common electrode voltage Vcom with the use of a programming unit, which may be easier for a test technician. Second, the calibration interface circuit 300 may be configured to provide high resolution adjustment of the common electrode voltage Vcom, thereby providing more control and accuracy in tuning such voltage. Third, the calibration interface circuit 300 uses a single-wire interface, which is desirable to reduce the number of pins on the LCD interface for performing this adjustment operation.

[0037] In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.